Form 1449 (Modified)	Atty Docket No.	Application No.:
	NSC1P275/P05654	10/650,215
Information Disclosure Statement By Applicant	Applicant: Mostafazadeh et al.	
	Filing Date	Group
(Use Several Sheets if Necessary)	08/27/2003	2811

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Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class	Filing Date
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*	B	6,607,941	12/19/03	Prabhu, et al.	438	113	1/11/2002
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Foreign Patent or Published Foreign Patent Application

Examiner Initial	No.	Document No.	Publication Date	Country or Patent Office	Class	Sub-class	Translation Yes	Translation No

Other Documents

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
	E	Reche, John, "*Wafer Thinning and Thru-Silicon Vias: The Path to Wafer Level Packaging*", Tru-Si Technologies, IEEE/CPMT Meeting, Santa Clara, CA, May 10, 2000, 42 Pages.
	F	Tru-Si Technologies, "*Thru Silicon Interconnects*", 33 Pages.
	G	Advanced Semiconductor Engineering Korea, Inc., "*CMOS Image Sensor*", http://www.asekr.com/doc/ASE_korea_Image_Sensor_overview.pdf, pages 4 and 5.

Examiner	Nitin Parekh	Date Considered	08-21-04

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.